SYSTEM ARCHITECTURE AND METHOD FOR SYNCHRONIZATION OF REAL-TIME CLOCKS IN A DOCUMENT PROCESSING SYSTEM

Abstract of the Disclosure

A system architecture and method are provided for synchronizing the slave clock of one or more resources with the master clock of a controller in a document processing system. The method includes: a) saving a value of the master clock (615); b) generating a discrete clock synchronization interrupt signal and distributing the interrupt signal to the resource(s) via the control bus (625); c) receiving the interrupt signal at each resource (630) and saving a value of the slave clock (640); d) sending a message to the controller via a network to request the value saved for the master clock (645); e) sending the value to the resource (660); f) receiving the value (665); and g) subtracting the value saved for the slave clock from the value saved for the master clock to determine an error value between the clocks (690) and using the error value in an adjustment algorithm to synchronize the slave clock with the master clock (695).

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